ABSTRACT OF THE DISCLOSURE

A circuit simulation apparatus is disclosed by which, even if an STS-N frame of an abnormal length is detected by a reassembly buffer, the frame length can be compensated for while preventing an overflow of the reassembly buffer. When an STS-(N×M) frame formed by multiplexing M STS-N frames formed from different channels is cellularized into ATM cells or M different STS-N frames assembled from ATM cells are multiplexed into an STS-(N×M) frame, an ATM cell sync signal and ATM cell data from a buffer section are outputted as a frame pulse signal and frame data from a reassembly section to a circuit termination section, and frame length compensation of the frame pulse signal and the frame data is performed by the reassembly section.